METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH FIELD ISOLATION REGIONS CONSISTING OF GROOVES FILLED WITH ISOLATING MATERIAL

The invention relates to a method of manufacturing a semiconductor device, wherein a surface of a silicon body is provided with an auxiliary layer of a material on which, during an oxidation treatment, a thicker layer of silicon oxide is formed than on the silicon of the silicon body, after which, at the location of field isolation regions to be formed, windows are formed in the auxiliary layer and grooves are formed in the surface of the silicon body, whereafter an oxidation treatment is carried out wherein the walls of the grooves and of the windows are provided with a layer of silicon oxide, but wherein it is precluded that the auxiliary layer adjacent to the windows is oxidized across the entire thickness, after which, successively, a layer of isolating material is deposited in a thickness such that the grooves and the windows are filled completely, a planarization treatment is carried out until the non-oxidized part of the auxiliary layer is exposed, and the non-oxidized part of the auxiliary layer is removed.

During the oxidation treatment, for example by heating the silicon body in an oxidizing atmosphere, the wall of the windows is provided with a layer of silicon oxide that is thicker than that formed on the wall of the grooves. Thus, next to the grooves, the layer of silicon oxide formed on the wall of the windows projects above the non-oxidized silicon of the silicon body. This isolating edge is removed over only a part of its thickness during the planarization treatment and during the etching away of the non-oxidized part of the auxiliary layer, as a result of which field isolation regions are formed whose isolating edge next to the grooves projects above the silicon of the silicon body next to the grooves. Thus, field isolation regions are formed having an isolating edge that projects above the active regions enclosed by field isolation regions.

After the field isolation regions have been provided in the silicon body, semiconductor elements having, inter alia, shallow pn-junctions extending parallel to the surface are formed in the active regions. During these further treatments, etch and cleaning processes are carried out wherein silicon oxide is etched away. If the field isolation regions were not provided with said edges, then the active regions could become exposed at the interface with the field isolation regions as a result of said etching away of silicon oxide. As a

result, the shallow pn-junctions would no longer be isolated. This is precluded by the edges formed at the field isolation regions, which edges overlap the active regions.

US 5,834,358 discloses a method of the type mentioned in the opening paragraph, wherein the surface of the silicon body is provided with a layer comprising 10^{19} to 10^{21} atoms per cc of comparatively heavily doped low-amorphous or polycrystalline silicon, which layer serves as an auxiliary layer. The doping may be p-type or n-type. The silicon body wherein the grooves are formed is lightly p-type doped with approximately 10^{16} atoms per cc. During oxidation, the comparatively heavily doped polycrystalline silicon is provided with a layer of silicon oxide that is thicker than that formed on the comparatively lightly doped monocrystalline silicon of the silicon body. The oxidation treatment is carried out at a temperature in the range of 800 to 950 °C in oxygen. A layer of silicon oxide is deposited as the isolating material. After the planarization treatment and removal of the non-oxidized part of the auxiliary layer of polycrystalline silicon, field isolation regions are formed having an edge that projects 20 to 50 nm above the active regions enclosed by field oxide.

The use of the comparatively heavily doped polycrystalline silicon as the material for the auxiliary layer has the drawback that, during the oxidation treatment, atoms of the dopant, such as phosphor or boron, may issue from the auxiliary layer and find their way into the grooves in the silicon body. During oxidation of the walls of the grooves, these atoms are then bound to each other in the interface between silicon oxide and the walls of the grooves. As a result, the isolating properties of the field isolation regions may be adversely affected.

It is an object of the invention to provide, inter alia, a method which does not have said drawback. To achieve this, the method in accordance with the invention is characterized in that a layer comprising silicon and germanium is applied as an auxiliary layer to the surface of the silicon body. During the oxidation treatment the silicon body is heated in a reaction chamber in an oxidizing gas, and silicon oxide and germanium oxide are formed during the oxidation of the auxiliary layer. The first oxide is stable, the second oxide evaporates in the reaction chamber. A layer of silicon oxide is formed on the walls of the windows in the auxiliary layer as well as on the walls of the grooves, the formation of silicon oxide on the walls of the windows in the auxiliary layer comprising silicon and germanium

taking place more rapidly than the formation of silicon oxide on the silicon of the walls of the grooves. As there is no dopant in the auxiliary layer, there is no risk that undesired atoms of a dopant are bound in the interface between silicon oxide and the walls of the grooves. The possible presence of germanium on the walls of the grooves has no influence on the isolating properties of the field isolation regions.

Preferably, on the surface of the silicon body a layer of $Si_xGe_{1-x-y}C_y$, where $0.70 < x < 0.95$ and $y < 0.05$, is provided as the auxiliary layer. Such a layer is stable at very high temperatures in the range of 1000 to 1100 °C. As a result, the desired layer of silicon oxide can be provided on the walls of the windows in the auxiliary layer and on the walls of the grooves at said very high temperatures. The oxidation treatment at such a high temperature can be carried out in a very short period of time.

During the oxidation treatment, wherein the walls of the grooves and of the windows are provided with a layer of oxide, it must be precluded that the auxiliary layer next to the windows is oxidized throughout its thickness. This can be readily achieved by applying the auxiliary layer in a sufficiently large thickness. This can also be achieved through an additional process step wherein a layer of silicon nitride is applied to the auxiliary layer, the windows being formed in the layer of silicon nitride as well as in the auxiliary layer. In this case, during the oxidation treatment the auxiliary layer is protected at the upper side by the layer of silicon nitride that is hardly subject to oxidation. The auxiliary layer is then provided with an oxide layer only at the location of the wall of the windows. The layer of silicon nitride has the additional advantage that it can be used as a stop layer during the planarization treatment. In order to be able to remove the non-oxidized part of the auxiliary layer, however, the layer of silicon nitride has to be removed first.

In order to be able to readily remove the non-oxidized part of the auxiliary layer from the surface, preferably prior to applying the auxiliary layer to the surface of the silicon body, said surface is provided with a layer of silicon oxide, and the windows are also formed in this layer. The auxiliary layer with silicon and germanium can be selectively etched from the layer of silicon oxide, so that damage to the surface of the silicon body by etching can be precluded.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiment(s) described hereinafter.

In the drawings:

Figs. 1 through 8 are diagrammatic, cross-sectional views of several stages in the manufacture of a semiconductor body by means of a first example of the method in accordance with the invention, and

Figs. 9 through 12 are diagrammatic, cross-sectional views of several stages in the manufacture of a semiconductor device by means of a second example of the method in accordance with the invention.

Figs. 1 through 8 are diagrammatic, cross-sectional views of several stages in the manufacture of a semiconductor device, wherein, in a silicon body 1, field isolation regions 2 are formed that enclose active semiconductor regions 3. In a first example of this method, a surface 4 of the silicon body 1 is provided with a 100 to 200 nm thick auxiliary layer 5. This auxiliary layer 5 is of a material on which, during oxidation, a thicker layer of silicon oxide is formed than on the silicon of the silicon body. In this example, an approximately 5 to 15 nm thick layer of silicon oxide 6 is provided between the auxiliary layer 5 and the surface.

On the auxiliary layer 5, a photoresist mask 7 having apertures 8 is formed in a customary manner, which apertures leave the auxiliary layer 5 exposed at the location of the field isolation regions 2 to be formed. Subsequently, as shown in Fig. 2, windows 9 are formed in the auxiliary layer 5, which comprise walls 10 extending transversely to the surface 4, and grooves 11 with walls 12 are formed in the surface 4 of the silicon body 1. If necessary, the photoresist mask 7 can be removed after the formation of the windows 9 in the auxiliary layer 5, whereafter the grooves 11 are etched using the auxiliary layer 5 as a mask. Preferably, the photoresist mask 7 is used, however, to form the windows 9 in the auxiliary layer 5 as well as the grooves 11 in the surface 4 of the silicon body 1 by means of a customary anisotropic etching treatment.

After the grooves 11 have been etched, an oxidation treatment is carried out wherein the silicon body is heated in an oxidizing gas mixture. In this oxidation treatment, as shown in Fig. 3, the walls 12 of the grooves 11 and the walls 10 of the windows 9 are provided with a layer of silicon oxide, i.e. the walls 12 of the grooves 11 are provided with a layer 13, the walls 10 of the windows 9 are provided with a layer 14. In the oxidation treatment, the auxiliary layer 5 is also provided, in this example, with a layer of silicon oxide 16 at the upper side 15. The auxiliary layer 5 is not converted to silicon oxide throughout its thickness; a layer 17 of the auxiliary layer remains.

As shown in Fig. 4, a layer of isolating material 18, in this example a layer of silicon oxide, is deposited in a thickness such that the grooves 11 and the windows 9 are filled completely. Subsequently, as shown in Fig. 5, a customary planarization treatment is carried out until the non-oxidized part of the auxiliary layer 17 is exposed. This part 17 is finally removed, as shown in Fig. 6.

In Fig. 7, the same situation is shown as in Fig. 6, but layers 13 and 18 are no longer shown individually. In this example both are made of silicon oxide. Finally, in Fig. 8, wherein the same situation is shown as in Fig. 7, a short customary etch treatment is carried out to remove the layer of silicon oxide 6 from the surface 4. As is shown in the Figure, an edge 19 of the field isolation region 2 projects above the active regions 3.

After the field isolation regions 2 have been formed in the silicon body 1, semiconductor elements (not shown) are formed in the active regions 3, said semiconductor elements having, inter alia, shallow pn-junctions which extend parallel to the surface 4. During these further operations, etching and cleaning processing are carried out wherein silicon oxide is formed and etched away. If the field isolation regions were not provided with the edges 19, then the active regions 3 could be exposed at their interface with the field isolation regions 2 by said operations. As a result, the shallow pn-junctions would no longer be isolated.

In this example, the surface 4 of the silicon body 1 is provided with an auxiliary layer 5 in the form of an approximately 100 to 200 nm thick layer comprising silicon and germanium. During the oxidation treatment the silicon body is heated in a reaction chamber to a temperature in the range of 1050 to 1160 °C in an oxygen-containing gas mixture for approximately 30 seconds, and silicon oxide and germanium oxide are formed during the oxidation of the auxiliary layer 5. The first oxide is stable, the second oxide evaporates in the reaction chamber. A layer of silicon oxide is formed on the walls 10 of the windows 9 in the auxiliary layer 5 as well as on the walls 12 of the grooves 11, the formation of silicon oxide on the walls 10 of the windows 9 in the auxiliary layer 5 comprising silicon and germanium occurring at a higher rate than the formation of silicon oxide on the silicon of the walls 12 of the grooves 11. As the auxiliary layer 5 does not contain a dopant, there is no risk that undesired atoms of a dopant are bound in the interface between the layer of silicon oxide 13 and the walls 12 of the grooves 11. The possible presence of germanium on the walls of the grooves does not influence the isolating properties of the field isolation regions 2.

Preferably, the surface 4 of the silicon layer 1 is provided with an auxiliary layer 5 in the form of a layer of $Si_xGe_{1-x-y}C_y$, where $0.70 < x < 0.95$ and $y < 0.05$. Such a layer is stable at very high temperatures in the range of 1000 to 1100 °C. As a result, the desired layer of silicon oxide 14 can be formed on the walls 10 of the windows 9 and the layer of silicon oxide 13 can be formed on the walls 12 of the grooves 11 at said very high temperatures. The oxidation treatment at such a high temperature can be carried out in a very short period of time, in this example approximately 30 seconds. The edge 19 shown in Fig. 8 then projects approximately 10 to 30 nm above the active regions 3.

In the example described herein, oxidation of the auxiliary layer 5 throughout its thickness was readily precluded in that said layer was provided in a sufficient thickness. The planarization treatment of the isolating layers 18 is interrupted when the non-oxidized part of the auxiliary layer 17 is exposed.

In the example of the method shown in Figs. 9 through 12, an approximately 50 nm thick layer of silicon nitride 20, as shown in Fig. 9, is applied to the auxiliary layer 5 having a thickness in this case of approximately 50 nm. The windows 9 are formed in the layer of silicon nitride 20 as well as in the auxiliary layer 5. As a result, during the oxidation treatment the auxiliary layer 5 is protected at the upper side by the layer of silicon nitride 20 which is hardly subject to oxidation. The auxiliary layer is then provided with a silicon oxide layer 14 only at the location of the wall 10 of the windows 9.

Fig. 10 shows the situation where a layer of silicon oxide 14 is applied to the walls 10 of the windows 9, and a layer of silicon oxide 13 is applied to the walls 12 of the grooves 11. Fig. 11 shows the situation after planarization of the layer of isolating material 18. In this example, the layer of silicon nitride 20 is used as a stop layer during the planarization treatment. After the planarization treatment, the layer of silicon nitride 20 is removed in a customary etch bath containing phosphoric acid, and subsequently the subjacent auxiliary layer 5 is removed in a customary etch bath containing nitric acid and hydrogen fluoride. Fig. 12 shows the structure thus formed, wherein the individual layers of silicon oxide 13, 14 and 18 are no longer shown.

As is indicated in both examples, the auxiliary layer 5 was applied to an approximately 5 to 15 nm thick layer of silicon oxide 6. As a result, the non-oxidized part of the auxiliary layer 17 can be readily removed from the surface 4. The auxiliary layer 5 can be selectively etched away from the silicon oxide layer 6 using a customary etch bath with nitric acid and hydrogen fluoride. As a result, damage to the surface 4 of the silicon body 1 by etching is precluded.